

REMARKS

Applicants thank the Patent Office for the careful attention accorded this Application and respectfully requests reconsideration in view of the Amendment above and remarks set forth below.

In response to the Office Action mailed March 17, 2008, Applicants have amended the Claim 43 to more particularly point out and distinctively claim the present invention over the prior art.

Claim 43 has been rejected under 35 USC Section 102 as being anticipated by US Patent Application Publication No. 2004/0180476 to Kazlas et al.

US Patent No. 2004/0180476 does not disclose or suggest a thin film transistor backplane as defined by Claim 43, having, *inter alia*, a gate insulating layer deposited over an array of gate electrodes and gate lines; a semiconducting channel layer deposited over the gate insulating layer; a contact layer deposited on and in contact with the semiconducting channel layer; and an array of source electrodes, drain electrodes, lines and pads fabricated on and in contact with the contact layer.

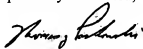
The Examiner has stated that these features are well known in the art, and refers to US Patent No. 6,175,394, which discloses flat panel display designs employing capacitatively coupled FETs for electrostatic discharge protection. However US Patent No. 6,175,394 does not disclose, teach or suggest how to make flexible thin film backplanes for use in electronic-ink based display devices.

Thus, Applicants believe rejection of Claim 43 is improper under 35 USC Section 102.

Favorable action is earnestly solicited.

The Commissioner is hereby authorized to any fee deficiencies to Deposit Account No. 16-1340.

Respectfully submitted,



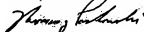
Dated: September 17, 2008

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Date: September 17, 2008